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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,830	11/15/2000	Toshiharu Furukawa	BUR9-2000-0029-US1	1095

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/713,830	FURUKAWA ET AL.-	
	Examin r	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- *If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.*
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10,12-43 and 45-47* is/are pending in the application.

4a) Of the above claim(s) *22-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10,12-21 and 45-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. The objection to claim 45 has been withdrawn in light of the amendment filed on September 12, 2003.

2. Applicant's arguments with respect to the patentability of claims 10, 12-21, and 45-47 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 45-47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "length" in claim 46 is used by the claim to mean the vertical dimension of the upper and lower portions of the gate, while the accepted meaning is

"the dimension in the direction of current flow between the source and the drain." The term is indefinite because the specification does not clearly redefine the term.

6. Although the applicant uses the word "length" in claim 46 to discuss the vertical dimensions of the upper and lower portions of the gate, the examiner believes that this term should be changed to thickness. In the semiconductor art, the term "length," when discussed with regard to a gate electrode, implies the dimension in the direction of current flow between the source and the drain. The examiner notes that the applicant has made use of the term "length" in this accepted manner within the current specification prior to the amendment filed on September 12, 2003. The examiner believes that claims 45-47 conflict with the specification and the accepted use of the term "length."

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10, 12, 16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. (USPN 6,306,710 B) in view of Hoshino et al. (USPN 6,528,848 B1) and further in view of Kohyama et al. (USPN 6,608,356 B1).

9. In referenced to claim 20, Long et al. (USPN 6,306,710 B1, hereinafter referred to as the "Long" reference) discloses a similar device. Figure 15 of Long illustrates a

FET with a gate comprising a first conductive material (labeled 230 in figure 13) and a second conductive material (labeled 286 in figure 14). The first conductive material (230) is polysilicon (column 4, lines 51-54) while the second conductive material (286) is a silicide (column 8, line 62); therefore they are different. The second conductive material (286) extends beyond the first conductive material (230) by a given distance. There is a first diffusion region (242) which is self-aligned to the first conductive material (230). There is a second diffusion region (252) which is defined by the second conductive material (286). The first diffusion (242) and the second diffusion region (252) are laterally offset by a distance equal to about the given distance. There is a spacer (262) along the sidewalls of the second conductive material (286). A third implant (labeled 272 in figure 13) is defined by the spacer. Long does not disclose making the silicide or second conductive material (286) thicker than the polysilicon or first conductive material (230). However the use of a silicide gate material which is thicker than the polysilicon gate material is well known in the art. Hoshino et al. (USPN 6,528,848 B1, hereinafter referred to as the "Hoshino" reference) discloses a gate electrode which has both silicide (7b) and polysilicon layers (7a) in figure 10. Hoshino discloses that the silicide (7b) is made thicker than the polysilicon (7a) in order to attain the benefit of a low gate resistance (column 16, lines 24-28). Kohyama et al. (USPN 6,608,356 B1, hereinafter referred to as the "Kohyama" reference) discloses that a low gate resistance is desirable (column 12, lines 7-12). In view of Hoshino and Kohyama, it would therefore be obvious to make the second conductive material thicker than the first conductive material.

10. In reference to claim 10, the first conductive material (230) is on a gate dielectric (labeled 202 in figure 13) on a substrate (204).

11. In reference to claims 12 and 16, the first conductive material comprises a first semiconductor material which is polysilicon (column 4, lines 51-54).

12. In reference to claim 19, the second conductive material comprises a silicide (column 8, line 62).

13. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. (USPN 6,306,710 B1) in view of Hoshino et al. (USPN 6,528,848 B1) and further in view of Kohyama et al. (USPN 6,608,356 B1) as applied to claim 12 above and further in view of Sagnes (USPN 5,998,289).

14. In reference to claim 13, Long does not disclose the use of germanium as a material in the gate electrode. However the use of germanium as a gate electrode is well known in the art. Sagnes (USPN 5,998,289) discloses that using germanium in the gate electrode provides the benefit of compatibility with both n and p type transistors which leads to a more efficient fabrication process (column 1, lines 26-32). It would therefore be obvious to utilize germanium in the gate electrode of Long in order to attain this benefit.

15. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. (USPN 6,306,710 B1) in view of Hoshino et al. (USPN 6,528,848 B1) and further in view of Kohyama et al. (USPN 6,608,356 B1) as applied to claim 12 above and further in view of Naruse et al. (USPN 5,356,821).

16. In reference to claim 14, Long does not disclose the use of a germanium compound (Ge_xSi_{1-x} with $0.5<x<1.0$) as a material in the gate electrode. However the use of a germanium compound (Ge_xSi_{1-x}) as a gate electrode is well known in the art. Naruse et al. (USPN 5,356,821, hereinafter referred to as the "Naruse" reference) discloses that using a germanium compound ($Si_{1-x}Ge_x$) in the gate electrode provides the benefit of lower resistance (column 7, lines 18-29). Naruse discloses an example where $x = 0.52$ (column 7, lines 18-21); thus meeting the limitation where $0.5<x<1.0$. Naruse also discloses that as germanium content increases, the resistance decreases (column 7, lines 22-25). It would therefore be obvious to utilize a germanium compound (Ge_xSi_{1-x} where $0.5<x<1.0$) in the gate electrode of Long in order to attain the benefit of lower resistance.

17. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. (USPN 6,306,710 B1) in view of Hoshino et al. (USPN 6,528,848 B1) and further in view of Kohyama et al. (USPN 6,608,356 B1) as applied to claim 20 above and further in view of Price et al. (USPN 4,570,328).

18. In reference to claim 15, Long does not disclose the use of polysilicon as the second conductive material in the gate electrode. However the use of polysilicon as material in a gate electrode is well known in the art. Price et al. (USPN 4,570,328, hereinafter referred to as the "Price" reference) discloses that using polysilicon in the gate electrode provides the benefit of compatibility with the high temperature processes which take place after the electrode and interconnect fabrication (column 1, lines 19-

34). It would therefore be obvious to utilize polysilicon as the second conductive material in the gate electrode of Long in order to attain this benefit.

19. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. (USPN 6,306,710 B1) in view of Hoshino et al. (USPN 6,528,848 B1) and further in view of Kohyama et al. (USPN 6,608,356 B1) as applied to claim 16 above and further in view of Kohyama et al. (USPN 6,608,356 B1).

20. In reference to claim 17, Long does not disclose the use of a refractory metal as the second conductive material in the gate electrode. However the use of a refractory metal as material in a gate electrode is well known in the art. Kohyama (USPN 6,608,356 B1) discloses that using a refractory metal such as tungsten in the gate electrode provides the benefit of a lower resistance. Kohyama also discloses that a low gate resistance is desirable (column 12, lines 7-12). In view of Kohyama, it would therefore be obvious to utilize a refractory metal, such as tungsten, as the second conductive material in the gate electrode of Long in order to attain this benefit.

21. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. (USPN 6,306,710 B1) in view of Hoshino et al. (USPN 6,528,848 B1) and further in view of Kohyama et al. (USPN 6,608,356 B1) as applied to claim 17 above and further in view of Kohyama et al. (USPN 6,608,356 B1).

22. In reference to claim 18, Long does not disclose the use of a refractory metal as the second conductive material in the gate electrode. However the use of a refractory metal as material in a gate electrode is well known in the art. Kohyama (USPN 6,608,356 B1) discloses that using a refractory metal such as tungsten in the gate

electrode provides the benefit of a lower resistance. Kohyama also discloses that a low gate resistance is desirable (column 12, lines 7-12). In view of Kohyama, it would therefore be obvious to utilize a refractory metal, such as tungsten, as the second conductive material in the gate electrode of Long in order to attain this benefit.

23. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. (USPN 6,306,710 B1) in view of Hoshino et al. (USPN 6,528,848 B1) and further in view of Kohyama et al. (USPN 6,608,356 B1) as applied to claim 13 above and further in view of Lin et al. (USPN 6,124,177).

24. So far as understood in claim 21, Long does not disclose the use of an air gap behind the spacer along a notched sidewall of the gate. However the use of an air gap in conjunction with a gate is well known in the art. Lin et al. (USPN 6,124,177, hereinafter referred to as the "Lin" reference) discloses that an air gap used in conjunction with the gate allows for a reduction in the Miller capacitance (column 6, lines 39-40). This leads to the benefit of a reduced gate delay (column 2, lines 23-32). In view of this advantage disclosed by Lin, it would therefore be obvious to use an air gap in conjunction with the gate electrode of Long.

25. Claims 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al. (USPN 6,306,710 B1) in view of Hoshino et al. (USPN 6,528,848 B1) and further in view of Kohyama et al. (USPN 6,608,356 B1) and further in view of Lin et al. (USPN 6,124,177).

26. So far as understood in claim 46, Long (USPN 6,306,710 B1) discloses a similar device. Figure 15 of Long illustrates a FET with a gate comprising a lower portion

(labeled 230 in figure 13) with first sidewalls and an upper portion (labeled 286 in figure 14) with second sidewalls. The first and second sidewalls are laterally offset. There are spacers (262) disposed on the second sidewalls. There is a first implant (242) disposed in the substrate (204) and aligned with the first sidewalls. There is a second implant (252) disposed in the substrate (204) and aligned with the second sidewalls. The first implant (242) and the second implant (252) are offset by a distance equal to about said lateral offset of the first and second sidewalls. Long does not disclose the use of an air gap along the second sidewalls of the gate and behind the spacers. However the use of an air gap in conjunction with a gate is well known in the art. Lin et al. (USPN 6,124,177, hereinafter referred to as the "Lin" reference) discloses a device (in figure 8) which uses an air gap behind the spacers along the lower portion of the gate. Lin discloses that an air gap used in conjunction with the gate allows for a reduction in the Miller capacitance (column 6, lines 39-40). This leads to the benefit of a reduced gate delay (column 2, lines 23-32). In view of this advantage disclosed by Lin, it would therefore be obvious to use an air gap along the second sidewalls of the gate and behind the spacers of the FET in Long. Long does not disclose making the upper silicide portion of the gate (286) thicker than the lower polysilicon portion of the (230). However the use of a silicide gate material which is thicker than the polysilicon gate material is well known in the art. Hoshino et al. (USPN 6,528,848 B1) discloses a gate electrode which has both silicide (7b) and polysilicon layers (7a) in figure 10. Hoshino discloses that the silicide (7b) is made thicker than the polysilicon (7a) in order to attain the benefit of a low gate resistance (column 16, lines 24-28). Kohyama (USPN

6,608,356 B1) discloses that a low gate resistance is desirable (column 12, lines 7-12). In view of Hoshino and Kohyama, it would therefore be obvious to make the second conductive material thicker than the first conductive material.

27. So far as understood in claim 45, the upper portion (286) of the gate extends beyond the lower portion (230) to provide a T-shaped gate.

28. So far as understood in claim 47, there is a third implant (labeled 272 in figure 13) disposed in the substrate (204) and aligned to the spacers (262).

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ